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METHOD OF FORMING FET SILICIDE GATE STRUCTURES INCORPORATING INNER SPACERS

Abstract

A method is provided for fabricating a gate structure for a semiconductor device in which the gate structure has an inner spacer. A replacement-gate process is used in which material is removed in a gate region to expose a portion of the substrate; a gate dielectric is formed on the exposed portion of the substrate; and an inner spacer layer is formed overlying the gate dielectric and the dielectric material. A silicon layer is then formed which overlies the inner spacer layer. The structure is then planarized so that portions of the silicon layer and inner spacer layer remain in the gate region. A silicide gate structure is then formed from the silicon; the silicide gate structure is separated from dielectric material surrounding the gate by the inner spacer layer. The semiconductor device may include a first gate region and a second gate region with an interface therebetween, with the inner spacer layer covering the interface. When the device has two gate regions, the process may be used in both gate regions, so as to produce sepa-

rate silicide structures, with an inner spacer separating the two structures.